REMARKS

Claims 1 - 4 are pending in the application.

Claims 1 - 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Sawa et al., (Sawa) US PAT 6,351,397.

The Applicants traverse the rejections and request recosndieration.

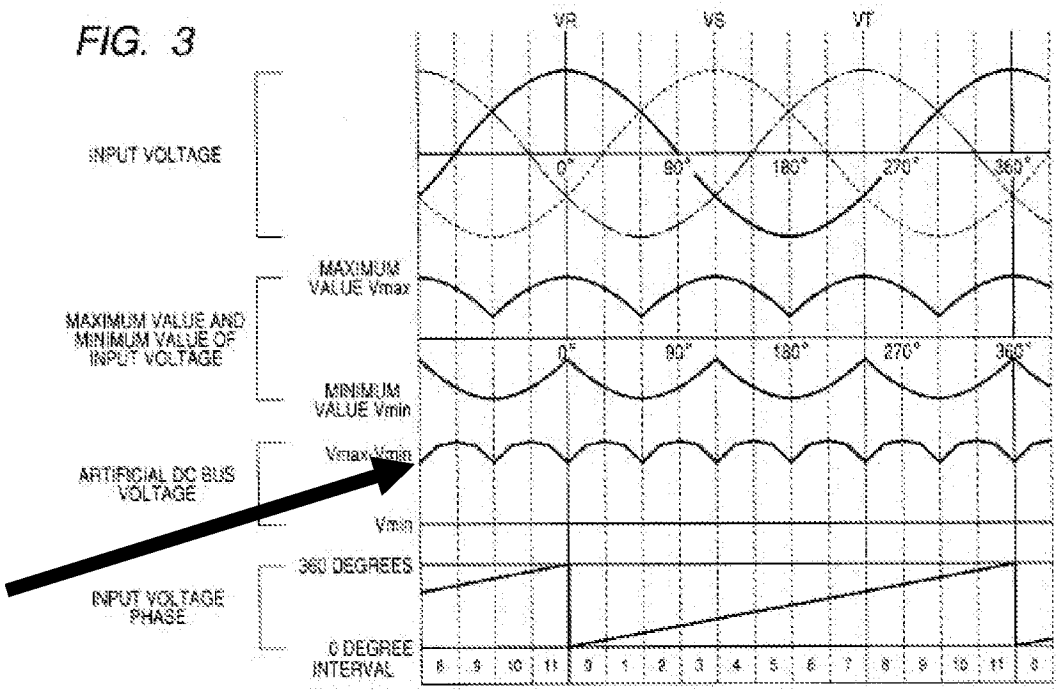
Claim Rejections Under 35 U.S.C. § 102(b)

Rejection of claims 1 - 4 under 35 U.S.C. 102(b) as being anticipated by Sawa et al..

In the previous response, filed on February 19, 2008, the Applicants noted that the cited reference Sawa is a patent owned by Yaskawa and its subject matter is discussed further in the background section of the present Specification. The Applicants also noted that the present invention provides a detection method that overcomes an error in the detected voltage that is caused due to a short circuit. In other words, the present invention is an improvement over Sawa and is aimed at solving a known error in the conventional art as disclosed in Sawa.

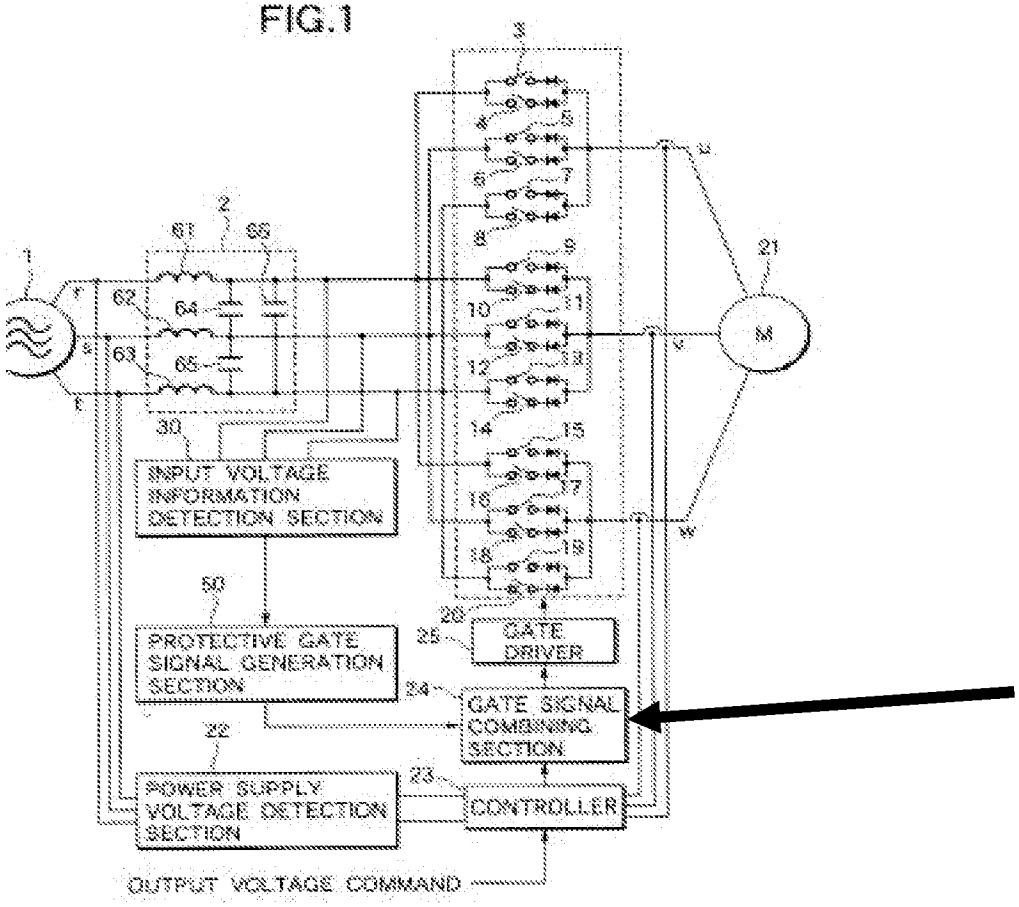
Specifically, the present invention (as recited in apparatus claim 3), *inter alia* requires an artificial DC bus voltage detector where the artificial DC bus voltage represents a magnitude of the three-phase AC power as a difference between a maximum value and a minimum value. For example, Fig. 3 of the present Specification shows the artificial DC bus voltage (as pointed to by the thick arrow shown below):

FIG. 3



The Examiner continues to maintain that item 22 of Sawa, which is described as a power supply voltage detection section, is equivalent to an artificial DC bus voltage detector of the present invention. Fig. 1 of Sawa is reproduced below. In alleged support of his position, the Examiner refers to col. 6, line 40 of Sawa. However, in this section, Sawa merely notes that the gate signal combining section 24 (shown with the thick arrow in Fig. 1 of Sawa, reproduced below) outputs the result of performing an OR operation on the gate signals G1yx, G1xy with G2yx, G2xy. The Applicants respectfully submit that, such an OR operation does not result in the artificial DC bus voltage of the present invention which represents the magnitude of the AC power as a difference between a maximum and a minimum value.

FIG.1



As is clear from Fig. 3 of the present Specification and the accompanying description, the artificial DC bus voltage is calculated by subtracting Vmin from Vmax. Such a value cannot be computed by simply performing an OR operation on G1yx and G2yx as the Examiner is alleging.

More importantly, a key aspect of the present invention is the computation of the ideal input voltage based on the above discussed artificial DC bus voltage and the phase. The Examiner again contends that that the gate signal combining section 24 of Sawa computes the ideal input voltage. However, as noted above, the gate signal combining section 24 merely performs the OR operation of the gate signals G1xy, G1yx with G2xy and G2yx. Such an OR

operation will not result in the idea input voltage. Therefore, Sawa does not disclose an artificial DC bus voltage detector or an ideal input voltage calculator.

Since Sawa does not disclose computing the ideal input voltage, it cannot be considered to be disclosing the input voltage upper and lower limit calculator that calculates a permissible width defined by the upper and lower limits for the ideal input voltage as required by the present invention. Likewise Sawa cannot be considered to be disclosing the voltage comparator which compares the voltage detected with the upper and lower limits for the ideal input voltage.

Specifically, paragraph [0097] of the present Specification notes that, in conventional technologies as in Sawa, input voltage values and phases are calculated directly based on power voltage. Therefore, a distortion as shown in Fig. 9 of the present Specification occurs in the waveform of an artificial DC bus voltage. On the other hand, in the present invention, the voltage value comparator compares the artificial DC bus voltage with the upper limit value and the lower limit value which define a specific width relative to the ideal input voltage value that is obtained. The artificial DC bus voltage is limited to the input voltage ideal value, thereby avoiding instantaneous distortions.

Importantly, Sawa is related to a method for protecting a PAM cycloconverter by preventing a surge voltage or an over current from causing at the output side upon shutting off the PWM cycloconverter.

In the method of Sawa, since the instantaneous value of the input voltage is used, there is a problem as follows. Namely, if a resonance or an instantaneous short-circuit is caused in the input voltage, an error is caused in the output voltage calculation, and an actual output voltage and a command voltage are different.

On the contrary, the present invention solves such a problem and has an object to provide a method for detecting an input voltage of a PWM cycloconverter so as to stably continue the operation relative to a sharp change in an input voltage.

An exemplar embodiment of the present invention includes the artificial DC bus voltage detection circuit (42), the input voltage effective value detection circuit (43), the ideal voltage calculator {44) and the input voltage upper and lower limit calculator (45). None of these components are included in Sawa. Because these structural components are not included in Sawa, it cannot continue operating stably relative to a sharp change in an input voltage.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." MPEP 2131 *citing Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The Examiner has not established anticipation of claim 3 based on Sawa at least because of the differences noted above.

Claim 1 is a method claim that includes limitations analogous to claim 3. Therefore, it is allowable at least for analogous reasons.

Claims 2 and 4 are dependent on claims 1 and 3 and are allowable at least for similar reasons.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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